WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a memory cell array including an array of memory cells, a plurality of bit line pairs each extending along a column of said memory cells, and a plurality of word lines each extending along a row of said memory cells;

a mode selection circuit for selecting either a normal operation mode or a test mode for said semiconductor memory device based on an external mode selection signal;

a command decoder for decoding a plurality of external commands in said normal operation mode to generate an internal control signal for each of said external commands, said internal control signal controlling operation of at least said memory cell array, said command decoder responding to a specified external signal in said test mode to generate a plurality of said internal control signals at specified consecutive timings; and

a controller for controlling operation of said semiconductor memory device based on said internal control signal.

2. The semiconductor memory device according to claim 1, wherein said plurality of internal control signals include an internal write signal for controlling a timing of inputting

write data to one of said bit line pairs, an internal precharge signal for controlling a timing of precharging said bit line pairs, and an internal activating signal controlling a timing of selecting one of said word lines.

3. The semiconductor memory device according to claim 2, wherein said plurality of internal control signals further include an internal read signal following said internal activating signal, said internal read signal controlling a timing of reading data from said one of said bit line pairs.

4. The semiconductor memory device according to claim 3, wherein said plurality of internal control signals further include another internal activating signal prior to said internal write signal, said another internal activating signal controlling a timing of selecting one of said word lines.

5. The semiconductor memory device according to claim 1, wherein said command decoder includes delay circuits for controlling said timings of said plurality of internal control signals.

6. The semiconductor memory device according to claim 1, wherein said specified external signal corresponds to a write command.